please enter amendment of spec dated 08/12/2004

Customer No.: 31561
Application No.: 10/707,668
Docket NO.: 09133-US-PA-1

→ enter claim amendment date 08/12/2004

In the Specification:

Please replace paragraph [0008] with the following amended paragraph:

[0008] Referring to Figure 1, Figure 1 is a schematic diagram, illustrating the structure of a conventional stacked gate flash memory (US patent 6214668). A conventional flash memory device is formed with a p-type substrate 100, a deep N-type well region 102, a P-type well region 104, a stacked gate structure 106, a source region 108, a drain region 110, a spacer 112, an inter-layer dielectric layer 114, a contact 116 and a conductive line 118. The stacked gate structure 106 comprises a tunnel oxide layer 120, a floating gate 122, a gate dielectric layer 124, a control gate 126 and a gate cap layer 128. The deep N-type well 102 is located in the P-type substrate 100. The stacked gate structure 106 is disposed on the substrate 100. The source region 108 and the drain region 110 are located beside the sides of the stacked gate structure 106 in the P- type substrate 100. The spacer 112 is disposed on the sidewall of the stacked gate structure 106. The P-type well region 104 is located in the N-type deep well region 102, extending from the drain region 110 to substrate 100 underneath the stacked gate structure 106. The interlayer dielectric layer 114 is disposed on the P-type substrate 100. The contact 116 penetrates through the inter-layer dielectric layer 114 and the substrate 100, short-circuiting the P-type well region 104 and the drain region 110. The conductive line 118 is disposed above the interlayer dielectric layer 114 and electrically connected with the contact 116.

Please replace paragraph [0009] with the following amended paragraph:

Electronic Version

Stylesheet Version v1.1.1

Description

[STRUCTURE OF FLASH MEMORY DEVICE AND FABRICATION METHOD THEREOF]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional application of, and claims the priority benefit of, U.S. application serial No. 10/065,554 filed October 30, 2002. now Patent No. 6,730,959

BACKGROUND OF INVENTION

[0002] Field of the Invention

[0003] The present invention relates to a structure of a non-volatile memory device and a method for fabricating the same. More particularly, the present invention relates to a structure of a flash memory device method and a method for fabricating thereof.

[0004] Description of Related Art

[0005] A flash memory device provides the property of multiple entries, retrievals and erasures of data. Moreover, the stored information is retained even electrical power is in-